Claims:

1. Method for monitoring event occurrences using a register having at least one capture bit with a plurality of storage bits, at least one logic operator, and a counter, said method comprising:

a) computing, at said at least one logic operator, a cumulative event signal from a plurality of input event signals indicative of respective occurrences of monitored events by the register;

b) capturing said cumulative event signal into the at least one capture bit of the register, wherein said cumulative event signal is received at a first frequency; and

c) shifting said stored cumulative event signal in said at least one capture bit to one of the plurality of storage bits in accordance with a shift rate signal, wherein said shift rate signal is received at a second frequency.

2. The method of claim 1, further comprising:

d) determining whether shifted information from the register is to effect counting by the counter.

3. The method of claim 2, wherein said second frequency is dependent upon a selectable time interval, and wherein said first frequency is different than said second frequency.

4. The method of claim 2, further comprising:

e) causing the counter to count if said shifted information from the register is indicative of an occurrence of a monitored event.

5. The method of claim 2, wherein said shifted information is received from the at least one capture bit of the register.

6. The method of claim 2, wherein said shifted information is received from one of the plurality of storage bits of the register.

7. The method of claim 1, further comprising:

d) determining whether information directly from the cumulative event signal is to effect counting by the counter.

8. The method of claim 7, further comprising:

e) causing the counter to count if said information directly from the cumulative event signal is indicative of an occurrence of a monitored event.

9. The method of claim 1, wherein said at least one logic operator comprises at least one of and an AND, NAND, OR, NOR, and exclusive OR logic operator.

10. Apparatus for monitoring event occurrences, comprising:

at least one logic operator for generating a single cumulative event signal from captured information from a plurality of event signals indicative of respective occurrences of monitored events;

a register having at least one capture bit with a plurality of storage bits for receiving said single cumulative event signal from said at least one logic operator, wherein said cumulative event signal is received at a first frequency; and

a shift rate controller for generating a shift rate signal, wherein said stored information in said at least one capture bit is shifted to one of the plurality of storage bits in accordance with said shift rate signal, wherein said shift rate signal is received by the register at a second frequency.

11. The apparatus of claim 12, further comprising:

a counter for determining whether shifted information from the register is to effect counting by said counter.

12. The apparatus of claim 11, wherein said second frequency is dependent upon a selectable time interval, and wherein said first frequency is different than said second frequency.

13. The apparatus of claim 11, wherein said counter counts if said shifted information from the register is indicative of an occurrence of a monitored event.

14. The apparatus of claim 11, wherein said shifted information is received from the at least one capture bit of said register.

15. The apparatus of claim 11, wherein said shifted information is received from one of the plurality of storage bits of said register.

16. The apparatus of claim 10, further comprising:

a counter for determining whether information directly from the cumulative event signal is to effect counting by said counter.

17. The apparatus of claim 16, wherein said counter counts if said information directly from the cumulative event signal is indicative of an occurrence of a monitored event.

18. The apparatus of claim 10, wherein said at least one logic operator comprises at least one of and AND, NAND, OR, NOR, and exclusive OR logic operator.

19. The apparatus of claim 10, further comprising:

a selector for selecting between a plurality of counting methods, where a first counting method determines whether shifted information from the at least one capture bit of the register is to effect counting by the counter, where a second counting method determines whether shifted information from one of the plurality of storage bits of the register is to effect counting by the counter, and where a third counting method determines whether information directly from the cumulative event signal is to effect counting by the counter.

20. A method for monitoring event occurrences from a plurality of functional processor units at a centralized location via a dedicated bus coupled between

said plurality of functional processor units and said centralized location, said method comprising:

receiving, at said centralized location, data indicative of cumulative events occurring at one of said functional processor units;

storing said data in a first temporary memory;

storing said data in a register based on a tag identifier affixed to said data, said tag identifier providing indicia of one of said plurality of functional processor units.

21. The method of claim 20 further comprising:

sending said data to a controller adapted to examine said data to determine whether said one of said plurality of functional processor units is to be reconfigured to operate in a different manner.

22. The method of claim 20 wherein said data comprises one of a pattern history and a count value.

23. The method of claim 20 further comprising:

performing an arithmetic-logic operation on said received data prior to storing said data in said register.

24. The method of claim 21, further comprising:

receiving, at said controller, said data collected from said digest controller;

comparing said collected data to a predetermined value;

generating an instruction message based on said comparison; and

sending said instruction message to said one of a plurality of functional processor units.

25. The method of claim 24 further comprising:

affixing an instruction tag to said instruction message, said instruction tag providing indicia of said one of a plurality of functional processor units.

26. The method of claim 24 wherein said sending step comprises sending said instruction message and affixed instruction tag over said dedicated bus.

27. The method of claim 21 wherein said reconfiguration of said one of said plurality of functional processor units comprises at least one of changing a manner of counting, changing a history pattern, changing at least one logic operator, initiating or terminating a count, changing at least one threshold, monitor different future event occurrences, and changing a clock rate.

28. The method of claim 20, wherein said data stored in said register is logically combined with a value originating from other functional processor units.

29. A digest collector for centrally monitoring event occurrences at a plurality of functional processor units, said digest collector comprising:

a bus latch, said bus latch having an input adapted for coupling to a dedicated bus that is coupled to said plurality of functional processor units, said bus latch for collecting data associated with at least one of said plurality of functional processor units;

a register file coupled to an output of said bus latch; and

control circuitry, coupled to said bus latch and said register file, said control circuitry for controlling transfer of said data associated with at least one of said plurality of function processor units to said register file.

30. The digest collector of claim 29, wherein said data comprises a tag identifying a particular functional processor unit.

31. The digest collector of claim 30, wherein said tag comprises indicia of whether to store said data in said register file.

32. The digest collector of claim 29 further comprising:

an arithmetic-logic unit (ALU) coupled to a first output of said bus latch and an input of said register file; and

a temporary register file coupled to second output of said bus latch, said temporary register file having an output coupled to said ALU.

33. The digest collector of claim 29 wherein said bus latch has an input coupled to a dedicated bus shared between said plurality of functional processor units.

34. The digest collector of claim 29 wherein an output of said register is coupled to a controller, said controller adapted to examine said data to determine whether said one of said plurality of functional processor units is to be reconfigured to operate in a different manner.